LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the claims of the present patent application.

1. (Currently Amended) A system for ~~detecting~~ counting occurrences of an edge of a data signal carried on an observability bus, the system comprising:

a first performance counter connected to receive said data signal, said first performance counter being operable to assert a trigger signal in a given clock cycle in response to detecting an assertion of said data signal in the previous clock cycle; and

a second performance counter connected to receive said data signal and said trigger signal, wherein said second performance counter ~~detects~~ counts an occurrence of said edge ~~based on said assertion of~~ when said data signal is asserted and ~~a logic level in~~ said trigger signal has a logic level that is a complement to a logic level associated with said assertion of said data signal.

2. (Original) The system as recited in claim 1, wherein said assertion of said data signal comprises an active high assertion.

3. (Original) The system as recited in claim 2, wherein said second performance counter inverts said trigger signal prior to detecting said logic level in said trigger signal.

4. (Original) The system as recited in claim 3, wherein said edge detected by said second performance counter comprises a rising edge.

5. (Original) The system as recited in claim 2, wherein said edge detected by said second performance counter comprises a falling edge.

6. (Cancelled)

7. (Currently Amended) The system as recited in claim [[6]] 1, wherein [[said]] the number of ~~detected~~ counted edges is employed in an average pulse width calculation.

8. (Original) The system as recited in claim 1, wherein said trigger signal comprises said data signal delayed by one cycle.

9. (Currently Amended) A method for ~~detecting~~ counting occurrences of an edge of a data signal carried on an observability bus, the method comprising:

receiving said data signal at a first performance counter;

asserting a trigger signal in a given clock cycle in response to detecting an assertion of said data signal in the previous clock cycle;

receiving said data signal and said trigger signal at a second performance counter; and

~~detecting~~ counting an occurrence of said edge ~~based on said assertion of~~ when said data signal is asserted and ~~a logic level in~~ said trigger signal has a logic level that is a complement to a logic level associated with said assertion of said data signal.

10. (Original) The method as recited in claim 9, wherein said operation of asserting a trigger signal further comprises asserting said trigger signal in response to detecting an active high assertion in said data signal.

11. (Original) The method as recited in claim 10, further comprising inverting said trigger signal prior to detecting said edge.

12. (Original) The method as recited in claim 11, wherein said operation of detecting said edge further comprises detecting a rising edge.

13. (Original) The method as recited in claim 10, wherein said operation of detecting said edge further comprises detecting a falling edge.

14. (Cancelled)

15. (Currently Amended) The method as recited in claim [[14]] 9, further comprising employing [[said]] the number of ~~detected~~ counted edges in an average pulse width calculation.

16. (Currently Amended) A system for ~~detecting~~ counting occurrences of an edge of a data signal carried on an observability bus, the system comprising:

means for receiving said data signal at a first performance counter;

means for asserting a trigger signal in a given clock cycle in response to detecting an assertion of said data signal in the previous clock cycle;

means for receiving said data signal and said trigger signal at a second performance counter; and

means for ~~detecting~~ counting an occurrence of said edge ~~based on said assertion of~~ when said data signal is asserted and ~~a logic level in~~ said trigger signal has a logic level that is a complement to a logic level associated with said assertion of said data signal.

17. (Original) The system as recited in claim 16, wherein said means for asserting a trigger signal further comprises means for asserting said trigger signal in response to detecting an active high assertion in said data signal.

18. (Original) The system as recited in claim 17, further comprising means for inverting said trigger signal prior to detecting said edge.

19. (Original) The system as recited in claim 18, wherein said means for detecting said edge further comprises means for detecting a rising edge.

20. (Original) The system as recited in claim 17, wherein said means for detecting said edge further comprises means for detecting a falling edge.

21. (Cancelled)

22. (Currently Amended) The system as recited in claim [[21,]] 16, further comprising means for employing [[said]] the number of ~~detected~~ counted edges in an average pulse width calculation.